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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,060	07/31/2003	Stephan Otis Broyles	AUS920030475US1	3508

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EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,060	BROYLES ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/25/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 24 are pending.

Response to Arguments

2. Applicant's arguments with respect to claim 1 – 24 have been considered but are moot in view of the new ground(s) of rejection. However, some parts of Applicant's arguments were found to be non-persuasive.

Applicant states that the claims describe a computer system that includes a processor card and a second processor card (See Applicant's Arguments; Page 14 Paragraph 5). However, the independent claims actually recite "said computer system including said processor card and ***a second resource card***" (emphasis added). A resource card is not the same as a processor card because a resource card is broader. A resource card is interpreted as a card that contains "any part of a computer system or a network, such as a disk drive, printer, or memory, that can be allotted to a program or a process while it is running" (See Microsoft Dictionary 5th Edition; Page 451 "resource"). However, a processor card is interpreted as a card that contains "the computational and control unit for a computer" (See Microsoft Dictionary 5th Edition; Page 132 "CPU").

Applicant also states that the Examiner's assertion that delaying a hardware reset request is not the same as placing a hardware reset request in a queue and does not teach a queue (See Applicant's Arguments; Page 14 Paragraph 6). Applicant does

not give any reasoning as to why delaying a hardware reset request does not teach a queue. The Examiner submits that delaying a hardware request does teach a queue. The claim does not limit the queue to a physical data structure resident in a computer memory and therefore does not read over a temporal queue. Since a queue is a list with a first-in-first-out structure, delaying a hardware reset request until after completion of a data transfer teaches the structure of a queue. Data transfer requests that were received before the hardware reset request are processed before the execution of the hardware reset. Therefore, delaying the reset request teaches a temporal queue structure.

Claim Rejections - 35 USC § 112 1st Paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1 – 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Amended independent claims 1, 9, and 17 recites "receiving, within said processor card ***from an application***, a hardware reset request that requests said processor card to reset said second resource card" (emphasis added). After a careful

review of the specification, the Examiner has determined that the specification does not describe receiving a hardware reset request in a processor card ***from an application*** (emphasis added). Therefore, the application contains new matter. Applicant's remarks have not pointed to a specific part of the specification that provides support for the limitation above. The specification describes receiving hardware reset requests and software communication requests (Figure 4), but does not describe where the hardware reset requests are received from. In the specification, Service Processor Card (Item 300) has a queue (Item 322) that holds software communication requests and hardware reset requests. The software communication requests are described as being generated by a software process (Specification; Page 12 Lines 19 – 25). However, it is not described in the specification where the hardware reset request is generated from.

Claim Rejections - 35 USC § 112 2nd Paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 – 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1 – 24, independent claim 1, 9, and 17 contradict the specification. The independent claims recite, "receiving, within said processor card from an application, a hardware reset request that requests said processor card to reset said second resource card," which is not supported by the specification (See new matter

rejection above). Therefore, it is not clear as to what generates the hardware reset request.

The Examiner has interpreted the hardware reset request to be received by the processor card and not limited as to where it is generated, as per the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 9, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,757,772 (hereinafter Ono).

As per claims 1, 9, and 17, Ono teaches a method of serializing hardware reset requests in a processor card, the processor card processing software requests in a serial order, the computer system including the processor card (Figure 1b Node "E") and a second resource card (Figure 1b Node "C"), the method comprising receiving in the processor card, a hardware reset request that requests the processor card to reset the second resource card (Col 4 Lines 37 – 42 "a change of bias voltage"); delaying the hardware reset request in the processor card (Col 7 Lines 50 – 54); processing requests in serial order, the hardware reset request being processed when all requests currently

being serviced have completed being serviced (Col 7 Lines 54 – 58); and resetting, by the processor card, the second resource card in response to the hardware reset request being processed (Col 8 Lines 20 – 25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 – 8, 10 – 16, and 18 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,757,772 (hereinafter Ono) in view of Applicants Admitted Prior Art (hereinafter AAPA, Citations of AAPA will be in reference to the publication of the current application, US Patent Application Publication 2005/0038917).

As per claims 2, 10, and 18, Ono teaches the system of serializing hardware reset requests of claims 1, 9, and 17 (see rejection of claims 1, 9, and 17 above) and wherein the computer system including a plurality of resource cards (Figure 1b Nodes "A" – "F") the second resource card included within the plurality of resource cards.

Ono does not teach wherein the processor card is coupled to the plurality of resource cards utilizing a single reset bus, and resetting, by the processor card utilizing the reset line, all of the plurality of resource cards simultaneously in response to a hardware reset.

However, AAPA teaches wherein a processor card is coupled to the plurality of resource cards utilizing a single reset bus (AAPA; Paragraph [0005]), and resetting, by the processor card utilizing the reset line, all of the plurality of resource cards simultaneously in response to a hardware reset (AAPA; Paragraph [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ono to include the single reset bus because doing so allows for resetting of all of the resource cards (AAPA; Paragraph [0005]).

As per claims 3, 11, and 19, Ono and AAPA also teach receiving software communication requests (AAPA; Paragraph; [0004]) and hardware reset requests (Ono; Col 4 Lines 37 – 42 "a change of bias voltage"), placing the software communication requests in a queue (AAPA; Paragraph [0004]) and delaying the hardware reset requests until all software communication requests have completed (Ono; Col 7 Lines 50 – 54).

As per claims 4 – 5, 12 – 13, and 20 – 21, Ono and AAPA also teach detecting whether the next request is a hardware reset request (Ono; Col 6 Line 66 – Col 7 Line 5); determining whether all of the plurality of resource cards have completed servicing of any pending software communication requests (Ono; Col 7 Lines 15 – 20, Col 7 Lines 50 – 58); and waiting to execute the hardware reset request until all of the plurality of

resource cards have completed servicing of any pending software communication requests (Ono; Col 54 – 58).

As per claims 6, 14, and 22, Ono teaches the system of serializing hardware reset requests of claims 1, 9, and 17 (see rejection of claims 1, 9, and 17 above).

Ono does not teach wherein the processor card coupled to the second resource card utilizing a hardware reset line; and resetting, by the processor card, the second resource card by pulling the hardware reset line high.

However, AAPA teaches wherein the processor card coupled to the second resource card utilizing a hardware reset line (AAPA; Paragraph [0005]); and resetting, by the processor card, the second resource card by pulling the hardware reset line high (AAPA; Paragraph [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ono to include the single reset bus because doing so allows for resetting of all of the resource cards (AAPA; Paragraph [0005]).

As per claims 7, 15, and 23, Ono teaches the system of serializing hardware reset requests of claims 1, 9, and 17 (see rejection of claims 1, 9, and 17 above).

Ono does not teach wherein the second resource card includes a microcontroller; the hardware reset request requesting the processor card to reset the microcontroller;

and resetting, by the processor card, the microcontroller in the second resource card in response to the hardware reset being processed.

However, AAPA teaches wherein the second resource card includes a microcontroller (AAPA; Paragraph [0004]); and resetting the microcontroller in the second resource card in response to the hardware reset being processed (AAPA; Paragraph [0005]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Ono to include the microcontroller resetting because doing so allows the microcode to get back into a running state from an undefined state (AAPA; Paragraph [0005]).

As per claims 8, 16, and 24, AAPA also teaches that each one of the resource cards includes a microcontroller, a memory (AAPA; Paragraph [0004]), and synchronization bits (AAPA; Paragraph [0006]); utilizing the synchronization bits to maintain information about current servicing of software communication requests by each one of the plurality of resource cards (AAPA; Paragraph [0006]); resetting the microcontroller and the synchronization bits in each one of the plurality of resource cards simultaneously in response to the receipt of the hardware reset request specifying one of a plurality of resource cards to reset (AAPA; Paragraph [0006]); and losing the information about current servicing of software communication requests by each one of the plurality of resource cards when the synchronization bits are reset (AAPA; Paragraph [0006]).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Microsoft Dictionary Fifth Edition – Used to describe different types of resource cards.
- JP11-205353-A – A Machine-Assisted Translation of JP 11-205353 that was used as a reference in the previous office action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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10/25/2006